IN THE U.S. PATENT AND TRADEMARK OFFICE

Appellants: Young-Doug KIM et al.

Application No.:   10/737,124

Art Unit: 2111

Conf. No.:   5936

Filed: December 17, 2003

Examiner: Khanh Dang

For: AN ARBITER, A SYSTEM AND A METHOD FOR
                     GENERATING A PSEUDO-GRANT SIGNAL

Atty. Dkt. No.:   8947-000074/US

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Randolph Building
401 Dulany Street
Alexandria, VA 22313
Mail Stop **Appeal Brief – Patent**

REPLY BRIEF

Sir:

In response to the Examiner's Answer mailed May 11, 2009,

Appellants hereby submit the following remarks. For the sake of brevity,

herein, Appellants will only respond to the Examiner's Answer as deemed

necessary. Appellants refer the Board to Appellants' Brief filed March 23,

2009, the contents of which are incorporated herein by reference, for a

recitation of the current rejection, a detailed discussion of example

embodiments of the present application, and the issues in this case.

I. The "pseudo grant signal" is a signal to grant bus ownership to a master.

In response to the arguments set forth in Appellants' Brief, the

Examiner's Answer states in-part at page 14:

> In response to Appellants' argument, at the outset, it is
> important to note that a "pseudo-grant signal" is not an
> actual grant signal from an arbiter. The "pseudo-grant signal"
> is a pre-grant signal provided to each of the requesting master
> units.

Appellants disagree this statement.

According to example embodiments, the pseudo grant signal

HGRANT *precedes* actual arbitration by the arbiter. But, contrary to the

above assertion, "[the pseudo grant signal] HGRANT signal is a signal to

grant bus ownership to a master." See, Appl. Spec. at p. 7, l. 12. Thus, the

statement that the pseudo grant signal HGRANT is "not an actual grant

signal from an arbiter" is not accurate.

As Appellants previously explained (see, e.g., Appl. Br. at 3), in

conventional arbitration mechanisms, grant and data transfer are

performed *after* actual arbitration of the bus. Example embodiments,

however, *modify the order of arbitration signals from the conventional order*

such that the pseudo grant signal *precedes* the arbitration. The target

information transfer regarding target slave devices also *precedes* the

arbitration so that the information contained in the data transfer may be

used in the arbitration decision.

While the pseudo grant signal does precede actual arbitration by the arbiter, the pseudo grant signal is indeed a grant signal from the arbiter in that it grants bus ownership to a master.

II. Claim 1 requires more than merely assigning concurrent ownership of a single data bus.

At page 14, the Examiner's Answer states in-part:

It is also important to note that in Kenny, assigning concurrent ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual arbitration **is interpreted as providing a pseudo bus grant signal by the arbiter to each master**.

At page 15, the Examiner's Answer further states:

Contrary to Appellants' argument, the arbiter 4 in Kenny "assigns a virtual channel to each master/slave pair requesting the data bus for data transfer between the master module and a slave module. Each virtual channel represents a timeslice on the bus and is owned by a separate master/slave pair, thereby permitting multiple master/slave pairs to have concurrent ownership of the singular data bus" (emphasis added). In other words, the arbiter 4 grants or bus ownership bus grant to the virtual channel of every requesting master before actual arbitration, wherein "data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate 'channel active' signal." It is clear that assigning concurrent ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual arbitration is interpreted as providing a pseudo bus grant signal by the arbiter to each master. In particular, in Kenny, a master module initializes bus access by asserting address and bus request signals on the bus 11. The arbiter 4 and the slave module detect the address and request signals asserted by the master module. The arbiter 4 then identifies the master module making the request, determines the master module's

priority, and grants a virtual channel. The virtual channel granted can be arbitrarily selected by an allocation procedure. [...] Kenny further discloses that "FIG. 9 is a timing diagram summarizing concurrent transactions of three virtual channels of the present invention." In addition, Kenny discloses that "[a]ll concurrent virtual channel owners wait for an access grant by arbiter 4 to data bus 2. Access to data bus 3 to a particular virtual channel occurs when arbiter 4 asserts the virtual channel's active signal (e.g., CHNLA ACTIVE). Note that in Fig. 9, because the priority of each requesting master (CPU, PCI Controller, Graphics Controller) is not pre-assigned, the arbiter 4 must resolve the priority between requesting masters, and grants virtual channels A, B, C to each requesting master based on priority of each requesting master, by asserting signal GNT CHLNA, signal GNTCHLNB, and signal GNTCHLNC, at times t1, t3, and t5. Fig. 9 is reproduced below:

Appellants appreciate these comments, but disagree.

Claim 1 does not merely require assigning concurrent ownership of a single data bus to each master by the arbiter before actual arbitration. Rather, to meet the limitations of claim 1, the arbiter 4 of *Kenny* must include "at least one interface for *generating pseudo-grant signals to all requesting master units beginning at the same time* and for *receiving transaction information from all requesting master units in response to the pseudo-grant signals.*" As previously argued, and again argued by Appellants below, Kenny does not disclose such an interface.

Referring to FIG. 5 of *Kenny*, at step 40 master module 5 initializes bus access by asserting an address and bus request signal (ADD/REQ) on the bus 11. *Kenny* at 6:62-65. After detecting the address and bus request signals asserted by the master module, the arbiter 4 identifies the

master module making the request, determines the master module's

priority, and grants a virtual channel at step 42. *Id.* at 7:1-3. The arbiter

4 grants the virtual channel by asserting by asserting GNT CHNL signals.

See, e.g., Kenny at 9:51-58. In Kenny, only <u>after</u> receiving the address and

bus request signal (ADD/REQ) does the arbiter 4 assert the virtual channel

grant signal to the requesting master module 5. Thus, the address and

bus request signal (ADD/REQ) is not received in response to the virtual

channel grant signal GNT CHNL, but rather the arbiter 4 in Kenny asserts

the virtual channel grant signal GNT CHNL in response to receiving the

address and bus request signal ADD/REQ.

This is further supported by FIG. 9A of *Kenny* (shown below), which

shows that the virtual channel grant is issued only <u>after</u> receiving an

address and bus request signal (ADD/REQ) signal from the master module.

FIG. 9A

FIG. 9

| FIG. 9A |
| FIG. 9B |

III. Kenny cannot provide virtual channel assignment signals to each master at the same time.

At page 15, the Examiner's Answer asserts:

The only difference between the claimed subject matter of that of Kenny is that Kenny does not explicitly disclose that the pseudo-grant signal is provided to each requesting master unit at the same time.

At page 18, the Examiner's Answer further states:

[...] Kenny also disclose that "[a]lternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere." Thus, it is clear that by using designating virtual channels and priorities for each module, the arbiter 4 does not have to determine assignment of the virtual channels to the modules (masters). As a result the arbiter 4 can send pseudo grant signals GNT CHNL to the requesting masters A, B, C at the same time.

Appellants disagree with this conclusion.

As seen above, the Examiner's Answer argues that "the arbiter 4 can send pseudo grant signals GNT CHNL to the requesting masters A, B, C at the same time." But, Appellants respectfully submit that this does not appear to be the case in Kenny.

According to example embodiments described in the present application, the arbiter 550 and the masters 510, 520, 530 shown in FIG. 7, for example, are connected in parallel. In example operation, the arbiter 550

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generates a pseudo grant signal HGRANT to each of the master units 510, 520, 530 at the same time. Each of the master units 510, 520, 530 then provides transaction information (e.g., HADDR signal, an HBURST signal, and/or an HWRITE signal) to the arbiter 550 in response to the pseudo grant signal HGRANT. By contrast, however, in Kenny the arbiter 4 is not connected to the other elements of the system in the same manner; that is, in parallel. See, e.g., Kenny at FIG. 1. Therefore, contrary to the above-assertion regarding Kenny, the arbiter 4 cannot send the virtual channel grant signals GNT CHNL to all requesting masters A, B, C at the same time. As shown in FIG. 9A of Kenny, these signals must be time-shifted relative to one another.

Further, at column 7, lines 5-13, Kenny states:

> Alternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere. At step 43, the assignment of virtual channel is entered into an "in service" table.

But, this portion of Kenny does not disclose, teach or suggest that pre-assigned priorities result in the issuance of the virtual channel grant signal GNT CHNL at the same time.

In Kenny, *the arbiter 4 assigns the virtual channel according to the master module's preassigned virtual channel and priority or to an allocation procedure. Kenny* at 7:36-40.

Regardless of whether the virtual channels are selected via an allocation procedure or configured with a fixed virtual channel having a pre-assigned priority, the virtual channel grant signals GNT CHNL are issued in the same manner; that is sequentially according to priority. The virtual channel grant signals GNT CHNL are not issued at the same time.

Further still, Appellants respectfully submit that the mere fact that the arbiter 4 in Kenny arguably could send virtual channel grant signals GNT CHNL to the requesting masters A, B, and C at the same time (which Appellants do not admit is the case for at least the reasons set forth above) is not sufficient to establish that such a modification would have been obvious to one of ordinary skill at the time of invention – especially given that such a modification changes the principle operation of the system in Kenny.

The system of *Kenny* issues virtual grant signals <u>sequentially</u> according to priority of the requesting master modules. If *Kenny* were to be modified as suggested by the Examiner, *the virtual channels would no longer be granted according to a master module's priority*, thereby significantly changing the principle operation of the system of *Kenny*; namely prioritizing bus ownership. Because the Examiner's suggested

modification would change the principle operation of *Kenny*, the teachings

of *Kenny* are not sufficient to render claim 1 *prima facie* obvious. MPEP §

2143.01(VI) ("If the proposed modification or combination of the prior art

would change the principle of operation of the prior art invention being

modified, then the teachings of the references are not sufficient to render

the claims *prima facie* obvious."), *In re Ratti*, 270 F.2d 810, 123 USPQ 349

(CCPA 1959).

Further still, the failure to generate pseudo-grant signals to all

requesting master units beginning at *the same time* is not the only

difference between claim 1 and *Kenny*. As previously argued, Kenny differs

from claim 1 in that the arbiter 4 of Kenny does not "[generate] pseudo-

grant signals [and receive] transaction information from all requesting

master units *in response to the pseudo-grant signals*." Claim 1 also

distinguishes over Kenny for other reasons as argued in Appellants' Appeal

Brief.

IV. The specifically cited portions of Kenny do not support the assertion that Kenny discloses the "transaction information" of claim 1.

At page 15, the Examiner's Answer further states:

> Further, in Kenny, <u>actual arbitration</u> performed by arbiter 4
> requires the information from all requesting masters. The
> "transaction information" (claim 1) from each master includes
> address of the target and/or priority of the target (ADD/REQ).

See at least column 5, lines 57-63; column 6, line 58 to column 7, line 65.

Regardless of whether the Examiner's statement is accurate, for the reasons set forth in Appellants' Brief and herein, *Kenny* still does not disclose or fairly suggest at least "*at least one interface for generating pseudo-grant signals to all requesting master units beginning at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signals*" as required by claim 1.

Further, page 15 of the Examiner's Answer directs Appellants' attention to column 5, lines 57-63 and column 6, line 58 to column 7, line 65 of *Kenny* to support the conclusion that Kenny discloses the "transaction information" of claim 1. But, Appellants submit that *Kenny* does not disclose or suggest any transaction information received by the arbiter 4 *in response to* pseudo grant signals generated by the arbiter 4, and thus, does not disclose or suggest the "transaction information" of claim 1.

Appellants have addressed the specific portions of *Kenny* in their Appeal Brief, and thus, for the sake of brevity will not repeat the same arguments herein. To be sure, however, column 5, lines 57-63 of Kenny states:

> Virtual channel control information (e.g., the addresses of the master/slave pair, their priority, and their virtual channel assignment) can be stored in a register in bus arbiter 4. Thus, bus arbiter 4 can signal grant of the data bus by either

asserting a dedicated "channel active" control signal for a given virtual channel, or providing identity bits of a virtual channel in dedicated bits of address bus 2.

At best, this portion of *Kenny* discloses that virtual channel control information can be stored at bus arbiter 4. This portion does not disclose or suggest that the virtual channel control information is received "from all requesting master units *in response to the pseudo-grant signals*" as is the case with the "transaction information" of claim 1.

Further, according to column 6, line 58 to column 7, line 65 of Kenny (which discusses FIGS. 5 and 6), only <u>after</u> receiving the address and bus request signal ADD/REQ does the arbiter 4 assert the virtual channel grant signal GNT CHNL to the requesting master module 5. Thus, the address and bus request signal ADD/REQ is not received in response to the virtual channel grant signal GNT CHNL, but rather the arbiter 4 in Kenny asserts the virtual channel grant signal GNT CHNL in response to receiving the address and bus request signal ADD/REQ.

FIG. 6 also shows that the address and bus request signal is issued by the master module *prior to* (not after or in response to) the virtual channel grant from the arbiter 4. Indeed, it is the virtual channel grant that is asserted by the arbiter 4 in response to the address and bus request signal from the master module, not vice versa.

V. In Kenny, at best the GNT CHNL signals are provided in response to the ADD/REQ signals, but not vice-versa.

At page 17, the Examiner's Answer further states:

> Kenny also discloses that the arbiter receives transaction information from all requesing master units in response to the pseudo-grant signals (after asserting GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the requesting master).

And, at page 19, the Examiner's Answer states:

> Further, in Kenny, <u>actual arbitration</u> performed by arbiter 4 <u>requires the information from all requesting masters</u>. The information from the master includes address of the target and/or priority of the target (ADD/REQ). See at least column 5, lines 57-63; column 6, line 58 to column 7, line 65. Thus, contrary to Appellants' argument, it is clear from Kenny, particularly from <u>Kenny's</u> Fig. 6 [...] that the next ADD/REQ is not independent. As a matter of fact, the next ADD/REQ would not be sent to the arbiter without reception of the pseudo grant GNT CHNL signal. In other words, ADD/REQs (transaction information) from requesting masters are sent to the arbiter in response to the pseudo-grant signals GNT CHNL.

Appellants disagree with the above conclusions.

Referring again to FIG. 6 of *Kenny*, upon detecting the address and bus request signal from the master module, the arbiter 4 asserts grant channel A signal GNT CHNLA on address bus 3 to assign a virtual channel to master module. *Kenny* at 7:34-7:37. After transmitting the virtual grant channel signal GNT CHNLA, the arbiter 4 returns to its initial state 47 to wait for the <u>next</u> address and bus request signal. *Id.* at 41-42. But, the next address and bus request signal received by the arbiter 4 is from a <u>different</u> master module (see, *Kenny* at FIG. 9A), and therefore, is

independent of – not in response to – the grant channel A signal GNT

CHNLA from the arbiter 4. Thus, contrary to the Examiner's assertion, the

arbiter 4 does not receive transaction information from a master module 5

in response to pseudo grant signals as required to meet the limitations of

claim 1. The mere fact that next address and bus request signal received

by the arbiter 4 in Kenny is subsequent in time to the issuance of the grant

channel A signal GNT CHNLA from the arbiter 4 does not disclose, suggest

or otherwise imply that they are dependent or in response to one another.

Indeed, as Appellants have argued, the two are independent.

At pages 20-21, the Examiner's Answer further argues the point

recited immediately above referring to FIG. 6 of Kenny. Specifically, with

regard to the following portion of FIG. 6:

MASTER A

GNT CHNL A
Assert
ADD/REQ on
address lines
46
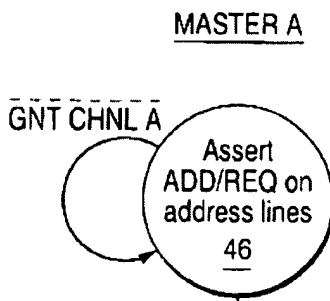
the Examiner's Answer states at page 21:

> As a [matter] of fact , as clearly shown in Fig. 6 [...], the
> ADD/REQ ("transaction information") is received in response
> to the pseudo grant signal GNT CHNL A.

Appellants respectfully disagree with this conclusion.

At column 7, lines 34-42, in describing FIG. 6 Kenny states:

> From initial state 47, arbiter 4 transitions to state 48 upon
> detecting master module A's assertion of the ADD/REQ signal,
> and asserts signal GNT CHNLA on address bus 3 to indicate
> assignment of a virtual channel ("virtual channel A") to master
> module A, according to either master module A's preassigned
> virtual channel and priority, or according to an allocation
> procedure, as discussed above. After asserting signal GNT
> CHNLA, arbiter 4 returns to its initial state 47 to wait for the
> next ADD/REQ signal.

As one can appreciate from this portion of Kenny, at best the arbiter

4 asserts signal GNT CHNLA in response to receipt of the ADD/REQ signal,

but not vice-versa. In direct contrast, however, in claim 1 transaction

information is received from all requesting master units *in response to* the

generated pseudo-grant signals.

At page 25, the Examiner's Answer states:

> In Kenny, it is important to distinguish between assigning
> virtual channels (pseudo grant) to masters by the arbiter 4 and
> actual arbitration between the masters performed by the
> arbiter 4, which requires the "transaction information" such as
> the address of the target and/or prioirty of the target.

The Examiner's Answer then goes on to assert that the ADD/REQ

signals in Kenny are indeed received in response to the virtual channel

grant signals GNT CHNL A.

Again, however, Appellants disagree. Specifically, in response,

Appellants direct the Board's attention to the arguments set forth in

Appellants' Brief on Appeal as well as the arguments set forth *supra.*

VI.   Claim 1 is not obvious over Kenny.

At pages 23 and 24, the Examiner's Answer states:

In response to Appellants' argument, at the outset, it is noted
that there is no evidence suggesting that "teachings of Kenny
are not sufficient to render claim 1 prima facie obvious." To the
contrary, <u>ample evidence set forth above proves that the
teachings of Kenny are clearly sufficient to render claim 1
obvious.</u>

Specifically, contrary to Appellants' argument, in addition to the
timing for pseudo-grant signals as shown in Fig. 9 above, Kenny
also disclose that "[a]lternatively, each subsystem may be
configured with a fixed virtual channel with a pre-assigned
priority. Pre-designating virtual channels and priorities for each
module simplifies processing by eliminating allocation
procedures and requiring arbiter 4 to merely match the I/O
address of the requesting master module to that master
module's pre-assigned virtual channel and pre-assigned
priority, referencing a table stored in a register of arbiter 4 or
elsewhere." Thus, it is clear that by using <u>pre-designating
virtual channels and priorities</u> for each module, the arbiter 4
<u>does not</u> have to determine assignment of the virtual channels
to the modules (masters). As a result the arbiter 4 can send
pseudo grant signals GNT CHNL to the requesting masters A, B,
C at the same time. Thus, it would have been obvious to one of
ordinary skill in the art at the time the invention was made to
generate pseudo-grant signals GNT CHLNA, GNT CHLN B, and
GNT CHLN C to all requesting masters <u>beginning at the same
time,</u> because by using a fixed virtual channel with a pre-
assigned priority for each of the requesting master, the arbiter 4
does not have to arbitrate between masters <u>resulting in
generating/providing pseudogrant signals to all requesting
masters at different starting time.</u> Since pseudo-grant signals
GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting
masters begin at the same time, it is clear that arbitration
latency can be further reduced, and as a result, the overall
performance of the entire system of Kenny is improved.

Initially, Appellants direct the Board's attention to the arguments set

forth above addressing similar rebuttal arguments.

Further, contrary to the above-statements, Appellants continue to submit that the Examiner's suggested modification would change the principle operation of *Kenny*, and therefore, the teachings of *Kenny* are not sufficient to render claim 1 *prima facie* obvious. MPEP § 2143.01(VI) ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."), *In re Ratti,* 270 F.2d 810, 123 USPQ 349 (CCPA 1959).[1]

VII. Appellants continue to challenge the Examiner's reliance on Wikipedia as evidentiary support for any conclusion.

At pages 31-32, the Examiner's Answer states:

Contrary to Appellants' argument, SDRAM "began its path to universal acceptance" in 1993 (see definition of SDRAM by Wikipedia, under "SDRAM history"). Thus, it is clear that SDRAM is well-known in the art at the time of Appellants' alleged invention. Further, while the Examiner agrees with Appellants that "Wikipedia is an open content encyclopedia," it is common knowledge that information provided by Wikipedia is verified by citations and references provided at the end of each Wiki document. As clearly discussed above and in the rejection of claim 11 and 12, memory such as SDRAM is old and well-known in the art since 1993. SDRAM is an improvement to standard DRAM in that it retrieves data alternately between two sets of memory. This eliminates the delay caused when one bank of addresses is shut down while another is prepared for reading. It's called "Synchronous" DRAM because the memory is synchronized with the clock speed that the computer's CPU bus speed is optimized for. The faster the bus speed, the faster the SDRAM can be. In

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[1] For a detailed explanation of this argument, Appellants direct the Board to Appellants' Brief on Appeal.

other words, SDRAM's timing is synchronized to the system clock. By running in sync to an external clock signal, SDRAM can run at the same speed as the CPU/memory bus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ SRAM in memory module 6 of Kenny, since the use of SDRAM for improving latency is old and well-known since 1993. Note also that in Kenny, the arbiter 4 comprises a slave interface directly interfacing and controlling/communicating with SDRAM memory 6 via SDRAM interface layers. Thus, it is clear that the slave controller interface in Kenny can be called "SDRAM controller interface."

Appellants continue to challenge the Examiner's citation of Wikipedia as sufficient to establish that a particular teaching was well-known in the art at the time of the invention. Although the Examiner now recognizes Wikipedia is an open content encyclopedia the contents of which can be edited by anyone, the Examiner's Answer continues to rely upon the open-content reference to support a conclusion. Appellants continue to challenge such reliance.

Moreover, Appellants also challenge the Examiner's mere comments or Official Notice on page 9 of the Final Rejection that the features of claims 11 and 12 would have been obvious. Regardless, however, claims 11 and 12 are patentable by virtue of their dependency from claim 1.

VIII. Further comments regarding the Examiner's Answer.

Because some of the rebuttal arguments set forth in the Examiner's Answer are similar and/or repetitive, for the sake of brevity Appellants

have combined and/or referred the Board's attention to similar arguments
where appropriate.

IX. Comments regarding the Examiner's Rebuttal to Parts D, E, and F of Appellants' Brief.

With respect to the rebuttal to Parts D, E, and F at pages 29 and 30
of the Examiner's Answer, Appellants direct the Board's attention to
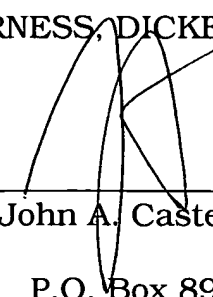Appellants' Brief as well as the arguments set forth *supra.*

CONCLUSION

In light of the foregoing arguments, Appellant respectfully requests
the Board to reverse the Examiner's rejection of claims 1-10 and 13-43.

The Commissioner is authorized in this, concurrent, and future
replies, to charge payment or credit any overpayment to Deposit Account
No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or
under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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